

# **RPI20** parallel interface

This data sheet contains an overview and specification of the Renishaw RPI20 parallel interface.

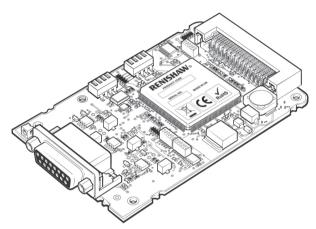
The RPI20 accepts differential analogue 1 Vpp sine/cosine signals, interpolates by 4096 and provides an output in parallel format with up to 36-bits of position data being available.

When used in combination with a double pass plane mirror interferometer system (PMI) (fundamental period of sinusoids is nominally 158 nm), this results in an LSB of 38.6 picometres at velocities of up to 1 m/sec.

The system architecture comprises a daughter board and 'industry standard' (VME) interface motherboards specifically designed to accommodate docking of either one or two (format dependent) daughter boards.

For multi-axis bus based architectures, the daughter board contains switches which allow each board to be assigned a unique address extending capability to up to seven axes. Additional switches enable selection of the LSB value and the direction sense to be changed.

Each daughter board contains four 36-bit wide addressable registers providing access to position, status and control information.



In the VME configuration, no connection is required to the P1 (VME interface) connector; all functions are accessed through the P2 connector.

Data timing is as shown in the timing diagram overleaf.

## Parallel interface performance

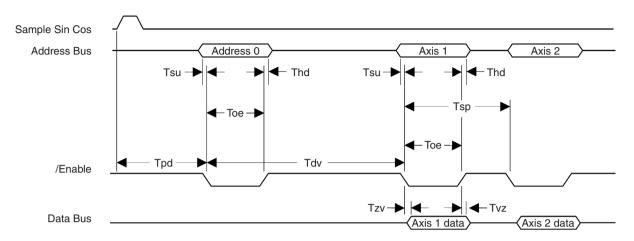
Resolution	38.6 pm (double pass plane mirror interferometer - PMI)				
	77.2 pm (single pass retroreflector interferometer - RRI)				
Maximum velocity	1 m/s (double pass plane mirror interferometer - PMI)				
	2 m/s (single pass retroreflector interferometer - RRI)				
Maximum update rate	4 MHz (single axis)				
	2.86 MHz (dual axis)				
	2.22 MHz (three axis)				
	Each additional axis will require a further 100 ns to read, assuming each axis is read in turn				
Data age uncertainty	<±10 ns				
SDE contribution (PMI)	<±0.5 nm (low bandwidth, velocities <50 mm/sec) >70% <120% signal strength				
	<±2 nm (full bandwidth, velocities <1 m/sec) >50% <120% signal strength				
User configurable features	Base address selection				
	LSB value (available selections with double pass PMI 38.6, 77.2, 154.4, 308.8 pm)				
	Direction sense				
Power supply required	5 V @ <500 mA for each parallel interface daughter board				
Connections	15-way D-type (interferometer/encoder input) (female on RPI20)				
	60-way JAE connector (36-bit parallel data) (male on RPI20)				
Operating environment					
Pressure	650 mbar to 1150 mbar	Normal atmospheric			
Humidity	0% to 95% RH	Non-condensing			
Temperature	10 °C to 40 °C				
Dimensions	110 mm x 72 mm (4.33 inches x 2.83 inches)				

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## Data transfer timing diagram



**Description:** Asserting address 000 causes all axes to record their current positions. Individual axis positions may then be read by addressing each axis position register in turn. The pipeline nature of the processing means that the analogue sine and cosine values used for interpolation are those sampled 80 ns ±10 ns (Tpd) before address 000 was asserted.

Parameter	Min	Nom	Max	Units	Comment
Tsu Toe Thd Tzv Tvz	10 50 10		35 35	ns ns ns ns	Set-up of address before /Enable falling edge Minimum period that /Enable must be active Period address to be held after /Enable rising edge /Enable to data valid Data valid to hi-impedence state
Tpd Tdv Tsp	70 140 100	80 150	90 160	ns ns ns	Propagation delay. The time before the /Enable that the sine / cosine signals are sampled Delay between /Enable falling edge and first valid position Time between sequential axis access

### Data available over the parallel bus

## Register 1: Position data

Register 1 of each interface module contains 36-bits of position data.

#### **Register 2: Status information**

Register contains system status information including the Lissajous coordinates (digitised sine and cosine), signal strength, error lines and switch settings. Arrangement of data is shown below.

<ul> <li>Digitised input cosine signal</li> </ul>	Bits 0 to 9
- Digitised input sine signal	Bits 10 to 19
- Signal strength	Bits 20 to 27
- Errors	Bits 28 to 31
- Switch settings	Bits 32 to 34

#### Register 3: Module reset

An individual module may be reset by accessing register 3 of the axis concerned. All cards may be simultaneously reset by accessing register 3 of address 0.

#### Register 4: Reserved for future expansion

Compliant with EU directive 2011/65/EU (RoHS)

